THE EMBODIMENTS OF THE INVENTION IN WHICH AN EXCLUSIVE PROPERTY OR PRIVILEGE IS CLAIMED ARE DEFINED AS FOLLOWS:

1. A data processing system comprising:

an input port for receiving input data; said input data comprising overhead control data and payload data;

a parallel array of data processing strips, said strip processing a slice of the payload data by using the overhead control data;

means for distributing input data from the input port to the data processing strips according to a distribution order;

an overhead control data delay block controlling input data reading on at least a pair of an i^{th} and a j^{th} data processing strips, such that corresponding input data is read on the j^{th} data processing strip after a predetermined delay from a time moment when corresponding input data is read on the i^{th} data processing strip, wherein i and j are integers assigned to the data processing strips according to the distribution order and j is greater than i;

means for collecting output data from the data processing strips according to a collection order; and

an output port for transmitting output data.

2. A data processing system comprising:

an input port for receiving input data; said input data comprising overhead control data and payload data;

a parallel array of data processing strips, said strip producing a new overhead control data by processing a slice of the payload data;

means for distributing input data from the input port to the data processing strips according to a distribution order;

means for transfer the new overhead control data from an i^{th} data processing strip to a j^{th} data processing strip, wherein i and j are integers assigned to the data processing strips according to the distribution order and j is greater than i;

means for collecting output data from the data processing strips according to a collection order; and

an output port for transmitting output data.

3. The data processing system according to claim 2, wherein the new overhead control data from the i^{th} data processing strip is incorporated into the processing of payload data on the j^{th} data processing strip.

4. The data processing system according to claim 3, further comprising:

storage means for storing an old first frame overhead control data, wherein the old first frame overhead control data is transmitted within the second frame;

a critical time signalling circuit; and

a comparator circuit, controlled by the critical time signalling circuit, for comparing the new overhead control data supplied by the data processing strip, with the old overhead control data supplied by the storage means.

wherein the critical time signalling circuit sends an enabling signal to the comparator, for enabling the comparison operation according to a predetermined comparison timing schedule.

5. In a digital optical network, a method of verifying an overhead value of a transmission frame processed at nodes of the network, the method comprising:

a) computing a local overhead value based on frame values received within a first transmission frame;

b) storing a transmitted first frame overhead values received within a second transmission frame; and

c) comparing the local overhead value and the transmitted first frame overhead value upon the reception of a comparison signal.

6. In a digital optical network, a method of verifying an overhead value of a transmission frame processed at nodes of the network, the method comprising:

a) receiving input data; said input data comprising overhead control data and payload data;

b) distributing input data from the input port to a parallel array of data processing strips according to a distribution order;

c) producing a new overhead control data by processing a slice of the payload data on one of the parallel array of data processing strips;

d) transferring the new overhead control data from an i^{th} data processing strip to a j^{th} data processing strip, wherein i and j are integers assigned to the data processing strips according to the distribution order and j is greater than i;

e) collecting output data from the data processing strips according to a collection order; and

f) transmitting output data.

7. The method according to claim 6, wherein producing a new overhead control data incorporates the overhead data from a second strip.

8. The method according to claim 6, further comprising the steps of:

storing an old first frame overhead control data, wherein the old first frame overhead control data is transmitted within the second frame;

enabling a comparison operation according to a predetermined comparison timing schedule; and

comparing the new overhead control data, with the stored old first frame overhead control data.

9. In a digital optical network, a method of overhead processing on a concatenated payload, the method comprising:

i) distributing the concatenated payload into a string of data slices according to a distribution order;

ii) determining an across-chip pair of data slices within said string, wherein the across-chip pair comprises data slices requiring overhead processing on separate integrated circuits; and

iii) transmitting overhead information from a first data slice in the across-chip pair to a second data slice in the across-chip pair by:

a) dividing the overhead information into a non-critical set and a critical set;

b) transmitting the non-critical set of overhead information away from a critical region, serially; and

c) transmitting the critical set of overhead information within the critical region, asynchronously.

10. A Bit Interleaved Parity-8 (BIP-8) computation system comprising:

a frame error check value computation block receiving first frame data from a frame processor, for computing new first frame BIP-8 values;

storage means receiving second frame data from the frame processor for storing old first frame BIP-8 values, wherein the old first frame BIP-8 value is transmitted within the second frame; and

a comparator circuit receiving data from the BIP-8 computation block, from the storage means and from a critical time signalling circuit, for comparing the new first frame BIP-8 values with the old first frame BIP-8 values,

wherein the critical time signalling circuit sends an enabling signal to the comparator, for enabling the comparison operation according to a predetermined comparison timing schedule.

11. The BIP-8 computation system in claim 10 where the BIP-8 values are B3 parity check bytes.

12. In a digital optical network, a method of computing a local frame error check values for a data slice of a transmission frames processed at nodes of the network, the method comprising:

a) computing a calculated local frame error check value based on frame values received within a first transmission frame;

b) storing a transmitted local frame error check values received within a second transmission frame; and

c) comparing the calculated local frame error check value and the transmitted local frame error check value upon the reception of a comparison signal.